I. The Prior Art Rejections

Claims 1, 4, and 7-8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Wong et al., hereinafter "Wong" ("Self-Aligned Top and Bottom Double-Gate MOSFET with a 25 nm Thick Silicon Channel"), IEDM 97, pp. 427; claims 2-3, 6, 9-16, and 18-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wong; and claims 5 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wong in view of Uesugi et al., hereinafter "Uesugi" (U.S. Patent No. 5,708,286). Applicants respectfully traverse these rejections based on the following discussion.

A. The 35 U.S. C. §102(b) Rejection Based on Wong

1. The Position In the Office Action

With respect to claims 1, 4, and 7-8, the Office Action states that Wong discloses a transistor comprising (Fig.4g) a channel region, a first gate on top of the channel region, a first gate dielectric below the first gate, a second gate dielectric above the second gate, and a second gate below the channel region. The Office Action states that the first gate comprises a different thickness than the second gate. The Office Action proposes that Wong discloses an isolation layer below the second gate. The Office Action states that the first and the second gates are

electrically separated from each other and that the first gate, the second gate, and the channel region form a planarized structure.

2. The Wong Reference

Wong discloses a fabrication method that attains the "ideal" double-gate MOSFET device structure. The top and bottom gates are inherently self-aligned to the source/drain. The source/drain is a fanned-out source/drain structure, which provides a low parasitic resistance. Channel silicon thickness is determined by a planar film deposition process with good uniformity control in principle. N-channel double-gate MOSFET's with a 25 nm thick silicon channel were successfully demonstrated by Wong.

3. Applicants' Response

One major distinction between the claimed invention and Wong is that the claimed invention includes first and second gates that are truly separate gates, while Wong discloses a gate material that surrounds the channel bridge. Therefore, Wong does not disclose truly separate gates that are defined by Applicants claims. Because the inventive gates are truly separate, independent claim 1 defines that they are ". . . electrically separated from each other" and independent claim 11 defines that the " . . . first gate comprises a different material than said

second gate." To the contrary, Wong forms the top gate and bottom gate in a single deposition process that allows the gates to surround the suspended silicon bridge. Therefore, the structure described in Wong cannot include gates that are electrically separated from each other or gates that are formed from different materials, as defined by Applicants' independent claims.

The device taught by Wong has a warped around gate. That is, the gate is "conformally deposited around the silicon bridge" (third line from the end of the Device Fabrication paragraph, page 428). Thus, the gate surrounds the silicon channel, which is shown as the suspended silicon bridge in Figures 4f and 4f'. Thus, the top portion of the surrounding gate is electrically connected to the bottom portion of the gate and the gates in Wong cannot be ". . . electrically separated from each other" as defined by independent claim 1 and Wong cannot provide a structure where the " . . . first gate comprises a different material than said second gate" as defined by independent claim 11.

Many benefits over the prior art are realized by the specific improvements of this invention. First, this invention deposits the top and bottom gates in two separate steps and creates top and bottom gates that are electrically separated, which results in several advantages. For example, the bottom gate may be used to control the threshold voltage, thereby allowing a mix threshold voltage (Vt) circuit for low power applications. This structure also allows for increases in the circuit density. When gates are electrically separated the double-gate MOSFET comprises a four terminal device with two input gates. Thus, a single device can be used to implement binary logic operations such as a NOR (nFET) or a NAND (pFET) cell. The

implementation of these binary logic functions would typically require two standard MOSFETs per cell. This increase in the circuit density also applies to analog circuits. For example, a mixer may be implemented by applying the oscillator voltage to one gate and the signal (data) voltage to the other gate.

Since the invention grows the top and bottom gates and respective gate dielectrics independently, the gates and gate dielectrics may be of different materials and different thicknesses. Also, different doping levels and doping species may be incorporated into each gate. Thus, asymmetric gates may be fabricated with the invention. To the contrary, since the gate in Wong's device is a warped around gate, which is deposited in one deposition step, both portion of the gate (bottom and top) are by definition of the same material and will have the same doping. The inventive asymmetric double-gate MOSFET is most useful for a mixed application where the gates are tied together to achieve speed and can be used separately to achieve low power and high density, e.g., for static random access memory (SRAM).

Also, the invention provides a structure that is planar, making it easier to connect the device. Devices with a very thin channel of about 3 to 5 nm thick may be required to obtain a good threshold voltage behavior. Fabricating suspended silicon bridges with a thin layer may reduce the overall yield. This invention supports the channel with a thick layer 22. Thus, the invention allows devices with a very thin channel to be fabricated and permits such devices to obtain a good threshold voltage behavior. The invention also utilizes a self-aligned silicide process which lowers the series resistance.

Further, Wong deposits the gate oxide simultaneously on either sides of the silicon bridge (which makes the device channel). Thus, by definition the gate insulator is of the same material and thickness. Wong cannot deposit the gate insulator in two separate steps since both bottom and top surfaces of the silicon channel (the suspended silicon bridge shown in figure 4f) are exposed at the time of the gate insulator deposition. In contrast, the invention allows the gate insulator to be deposited in two separate steps, thus different material and thicknesses can be used.

Also, Wong's device is physically connected to the substrate as can be seen in Figures 4f and 4g. The drain (Fig. 4f) or the source (Fig. 4g) is connected to the substrate through a seed window. In the invention, both source and drain are isolated from the substrate by an insulator layer.

Therefore, since Wong discloses a gate material that surrounds the channel bridge, it cannot teach or suggest gates that are ". . . electrically separated from each other" as defined by independent claim 1. Therefore, independent claim 1 is patentable over Wong. Further, dependent claims 4, 7, and 8 are similarly patentable, not only by virtue of their dependency from patentable independent claim 1, but also by virtue of the additional features of the invention they define. In view the forgoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

B. The 35 U.S. C. §103(a) Rejection Based on Wong

1. The Position In the Office Action

Regarding claims 2-3 and 12-13, the Office Action states that Wong teaches substantially the entire claimed structure, as explained in claim 1 above, except that the first gate comprises a different doping concentration than the second gate. The Office Action contends, however, that it is well known in the art to select the concentration of gate electrode to adjust a threshold voltage in the transistor. The Office Action recites that if the first gate electrode has a lower concentration than the second gate electrode, a threshold voltage of the first gate is lower than that of the second gate. Thus, the Office Action concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed Wong's first and second gate to have different concentrations since the different concentrations of gate electrode provides the different threshold voltages in device.

The Office Action argues regarding claims 6, 9, and 15, that although Wong does not teach that the first gate and first gate dielectric layer comprise a different material than the second gate and second gate dielectric layer, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the dielectric layer, having the materials as claimed, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design

choice. The Office Action cites In re Leshin, 125 USPQ 416.

Regarding claims 10 and 16, the Office Action argues that, although Wong does not teach the first gate dielectric layer comprise a different thickness than the second gate dielectric layer, the selection of thickness of various layers in device is an obvious design choice, therefore held within ordinary skills in the art.

Regarding claims 11, 14, and 18-20, the Office Action states that Wong discloses a transistor comprising (Fig.4g), a channel region, a first gate on top of the channel region, a first gate dielectric below the first gate, a second gate dielectric above the second gate, a second gate below the channel region (wherein the first gate comprises a different thickness than the second gate), and an isolation layer below the second gate, where the first and the second gate are electrically separated from each other, and the first gate, the second gate and the channel region form a planarized structure. The Office Action also refers to the section titled Device Fabrication of Wong. The Office Action recites that Wong does not explicitly teach the first gate comprises a different material than the second gate. The Office Action proposes that this feature is obvious for the same reasons as given for the rejection of claim 6.

2. **Applicants' Response**

As explained above, an important distinction is that the claimed invention includes first and second gates that are truly separate gates, while Wong discloses a gate material that

surrounds the channel bridge. Therefore, Wong does not disclose truly separate gates that are defined by Applicants claims. Because the inventive gates are truly separate, independent claim 1 defines that they are "... electrically separated from each other" and independent claim 11 defines that the "... first gate comprises a different material than said second gate." To the contrary, Wong forms the top gate and bottom gate in a single deposition process that allows the gates to surround the suspended silicon bridge. Therefore, the structure described in Wong cannot include gates that are electrically separated from each other or gates that are formed from different materials, as defined by Applicants' independent claims.

The device taught by Wong has a warped around gate. That is, the gate is "conformally deposited around the silicon bridge" (third line from the end of the Device Fabrication paragraph, page 428). Thus, the gate surrounds the silicon channel, which is shown as the suspended silicon bridge in Figures 4f and 4f'. Thus, the top portion of the surrounding gate is electrically connected to the bottom portion of the gate and the gates in Wong cannot be "... electrically separated from each other" as defined by independent claim 1 and Wong cannot provide a structure where the "... first gate comprises a different material than said second gate" as defined by independent claim 11.

Many benefits over the prior art are realized by the specific improvements of this invention. First, this invention deposits the top and bottom gates in two separate steps and creates top and bottom gates that are electrically separated, which results in several advantages. For example, the bottom gate may be used to control the threshold voltage, thereby allowing a

mix threshold voltage (Vt) circuit for low power applications. This structure also allows for increases in the circuit density. When gates are electrically separated the double-gate MOSFET comprises a four terminal device with two input gates. Thus, a single device can be used to implement binary logic operations such as a NOR (nFET) or a NAND (pFET) cell. The implementation of these binary logic functions would typically require two standard MOSFETs per cell. This increase in the circuit density also applies to analog circuits. For example, a mixer may be implemented by applying the oscillator voltage to one gate and the signal (data) voltage to the other gate.

Since the invention grows the top and bottom gates and respective gate dielectrics independently, the gates and gate dielectrics may be of different materials and different thicknesses. Also different doping levels and doping species may be incorporated into each gate. Thus, asymmetric gates may be fabricated with the invention. To the contrary, since the gate in Wong's device is a warped around gate, which is deposited in one deposition step, both portion of the gate (bottom and top) are by definition of the same material and will have the same doping. The inventive asymmetric double-gate MOSFET is most useful for a mixed application where the gates are tied together to achieve speed and can be used separately to achieve low power and high density e.g. for static random access memory (SRAM).

Also, the invention provides a structure that is planar, making it easier to connect the device. Devices with a very thin channel of about 3 to 5 nm thick may be required to obtain a good threshold voltage behavior. Fabricating suspended silicon bridges with a thin layer may

reduce the overall yield. This invention supports the channel with a thick layer 22. Thus, the invention allows devices with a very thin channel to be fabricated and permits such devices to obtain a good threshold voltage behavior. The invention also utilizes a self-aligned silicide process which lowers the series resistance.

Further, Wong deposits the gate oxide simultaneously on either sides of the silicon bridge (which makes the device channel). Thus, by definition the gate insulator is of the same material and thickness. Wong cannot deposit the gate insulator in two separate steps since both bottom and top surfaces of the silicon channel (the suspended silicon bridge shown in Figure 4f) are exposed at the time of the gate insulator deposition. In contrast, the invention allows the gate insulator to be deposited in two separate steps, thus different material and thicknesses can be used.

Also, Wong's device is physically connected to the substrate as can be seen in Figures 4f and 4g. The drain (Fig. 4f) or the source (Fig. 4g) is connected to the substrate through a seed window. In the invention, both source and drain are isolated from the substrate by an insulator layer.

Therefore, since Wong discloses a gate material that surrounds the channel bridge, it cannot teach or suggest gates that are ". . . electrically separated from each other" as defined by independent claim 1 or that the " . . . first gate comprises a different material than said second gate" as defined by independent claim 11. Therefore, independent claims 1 and 11 are patentable over Wong. Further, dependent claims 2, 3, 6, 9, 12-16, and 18-20 are similarly patentable, not

only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view the forgoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

C. The 35 U.S. C. § 103(a) Rejection Based on Wong in view of Uesugi

1. The Position In the Office Action

With regard to claims 5 and 17, the Office Action states that Wong applies to claims 1 and 11 as stated above. The Office Action argues that although Wong fails to teach that the first conductive contact of first gate and the second conductive contact of second gate are coplanar, Uesugi teaches in Fig. 1 and Col.7, lines 42-46, the first conductive contact (80) of first gate (60) and second conductive contact (90) of second gate (30) are coplanar. Therefore, the Office Action concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Uesugi with Wong's device in order to reduce a manufacturing processing.

2. The Uesugi Reference

Uesugi discloses a vertical semiconductor device having an insulated gate structure that makes use of a double-gate structure. The double-gate structure dramatically reduces the channel resistance, JFET resistance, and epitaxial resistance of the on-resistance of the power MOSFET, and implements an adequate breakdown voltage due to the effect of gate bias. In principle, a first gate and a second gate having mutually facing portions are driven synchronously. This causes first and second channels to be formed in correspondence with the first and second gates, and the currents flowing through these first and second channels form the on-current for this vertical structure power device.

3. Applicants' Response

As explained above, Wong does not disclose truly separate gates that are defined by Applicants' claims. Because the inventive gates are truly separate, independent claim 1 defines that they are ". . . electrically separated from each other" and independent claim 11 defines that the " . . . first gate comprises a different material than said second gate." To the contrary, Wong forms the top gate and bottom gate in a single deposition process that allows the gates to surround the suspended silicon bridge. Therefore, the structure described in Wong cannot

include gates that are electrically separated from each other or gates that are formed from different materials, as defined by Applicants' independent claims.

Uesugi does not cure the deficiencies of Wong. More specifically, Uesugi does not teach the double-gate structure defined by the claimed invention. The claimed invention includes a single channel between an upper gate and a lower gate. To the contrary, with the structure in Uesugi, two channel regions "Ch1" and "Ch2" are formed, one adjacent the first gate and another adjacent the second gate. Therefore, Uesugi is not in the same art field as the invention or Wong (because Uesugi teaches multiple channel regions) and is not properly combinable with Wong to arrive at the claimed invention.

In addition, Uesugi does not teach or suggest the claimed "isolation layer below said second gate," as defined by independent claims 1 and 11. While Uesugi discloses a gate insulator GIS2 that surrounds the lower gate 30, this is not analogous to the claimed "isolation layer." An isolation layer completely separates the gate from any bias within an underlying substrate. To the contrary, a gate insulator is extremely thin and allows the substrate to have some biasing effect on an adjacent gate. Therefore, the usage of the term "isolation" in the claimed invention is an important feature that distinguishes the gate insulator "GIS2" of Uesugi from the claimed invention.

As shown above, Uesugi is not properly combinable with Wong and cannot render either independent claim 1 or 11 obvious. Further, even if one ordinarily skilled in the art would have combined Uesugi and Wong, the proposed combination would not teach or suggest the invention

because neither reference teaches or suggests a dual gate structure where the gates are truly separate, and are "... electrically separated from each other" (claim 1) and that the "... first gate comprises a different material than said second gate" (claim 11). Therefore, independent claims 1 and 11 are patentable over the proposed combination of Uesugi and Wong. Further, dependent claims 5 and 17 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-20, all the claims presently being examined in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time. Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

S.N. 09/612,260
Response Under 37 CFR 1.116

Please charge any deficiencies in fees and credit any overpayments to Attorney's Deposit Account Number 50-0510.

Respectfully submitted,

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